DLP® PICO™ PROCESSOR DPP1505 DATA SHEET

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TEXAS INSTRUMENTS
POST OFFICE BOX 655474 DALLAS, TEXAS 75265

DRAWING NUMBER	REVISION	
2510327	A	Sheet 1

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Revision History

Rev	Section	Revisions
A	All	Preliminary release

TEXAS INSTRUMENTS
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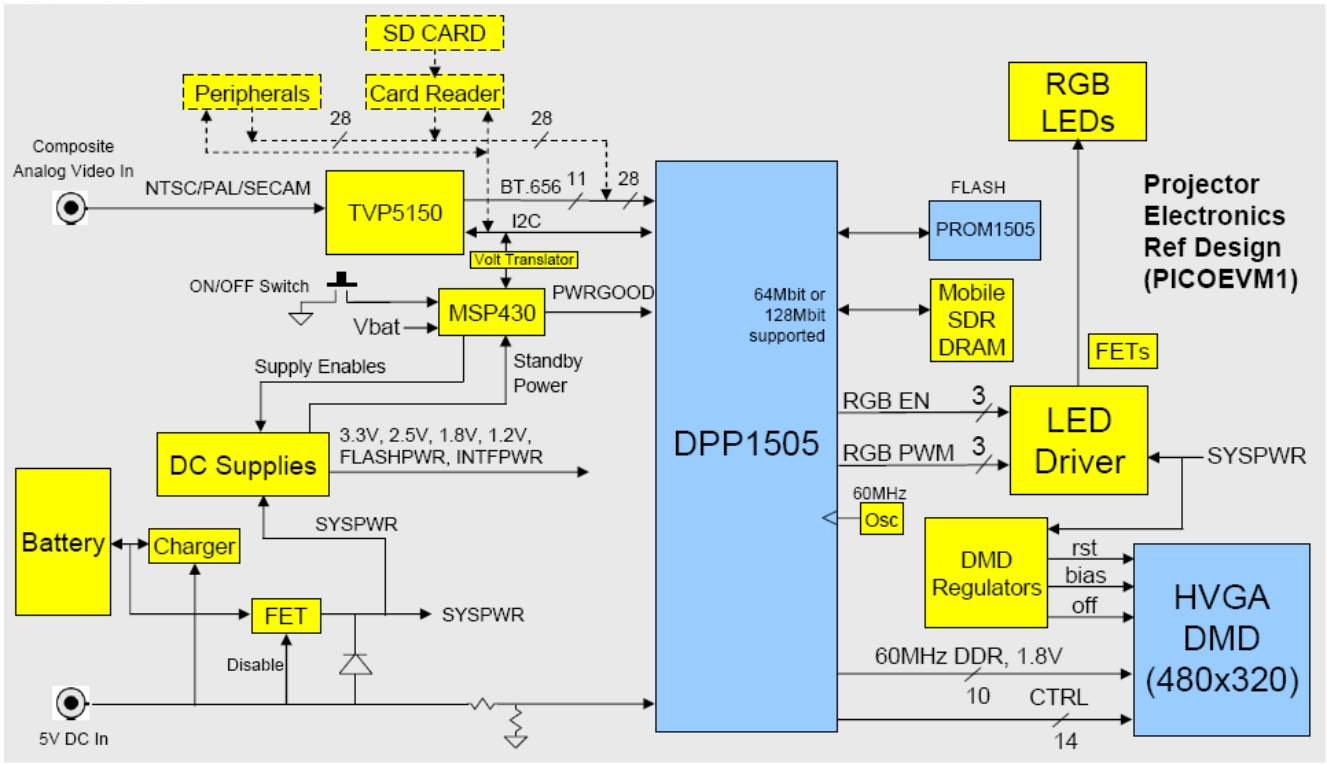
DRAWING NUMBER	REVISION	
2510327	A	Sheet 3

- **Input Pixel Interfaces:**
  - **Single 24-bit input port (RGB or BT656-YUV) with Pixel Clock support up to 30 MHz**
  - **Input image size 320x240 (QVGA), 480x320 (HVGA), or 640x480 (VGA)**
  - **Portrait or Landscape inputs**
  - **Three RGB input color bit-depth options: RGB888, RGB666, RGB565**
- **Supports 1Hz to 60Hz Frame Rates**
- **60MHz Double Data Rate (DDR) DMD Interface**
- **Serial Control Interface for device configuration**
- **Pixel Data Processing:**
  - **Color Space Conversion**
  - **Chroma Interpolation for 4:2:2 to 4:4:4 conversion**
  - **Color Coordinate Adjustment**
  - **Image resizing (Scaling)**
  - **Deinterlacing via Field scaling**
  - **Frame Rate Conversion**
  - **LED Current Control Adjustment**
  - **Programmable Degamma**
  - **Spatial-Temporal Multiplexing (dithering)**
  - **Automatic Gain Control**
  - **Built in Test Patterns**

- **Full functionality support for 480x320 DMD (HVGA)**
- **DMD data formatting**
- **Mode processor (processor for controlling the LEDs and DMD mirrors)**
- **Pulse-Width-Modulation (PWM) for Mirrors:**
  - **Auto Micro-mirror Parking at Power Down**
  - **24-bit bit-depth on DMD**
- **External Memory Support:**
  - **100MHz SDR SDRAM**
- **Serial FLASH Interface**
- **System Control:**
  - **Programmable Splash Screens**
  - **Programmable LED Duty Cycles**
  - **Programmable LED Currents**
  - **DMD Power and Reset Driver Control**
  - **DMD horizontal and vertical Image Flip**
  - **Image rotation on the DMD**
  - **Programmable power-up configuration defaults**
  - **Built in Test Pattern Generation**
- **JTAG with Boundary Scan Test Support**
- **Packaged in 256-Pin Ultra Fineline Ball-Grid Array (uBGA)**

Typical Projector Application



Description

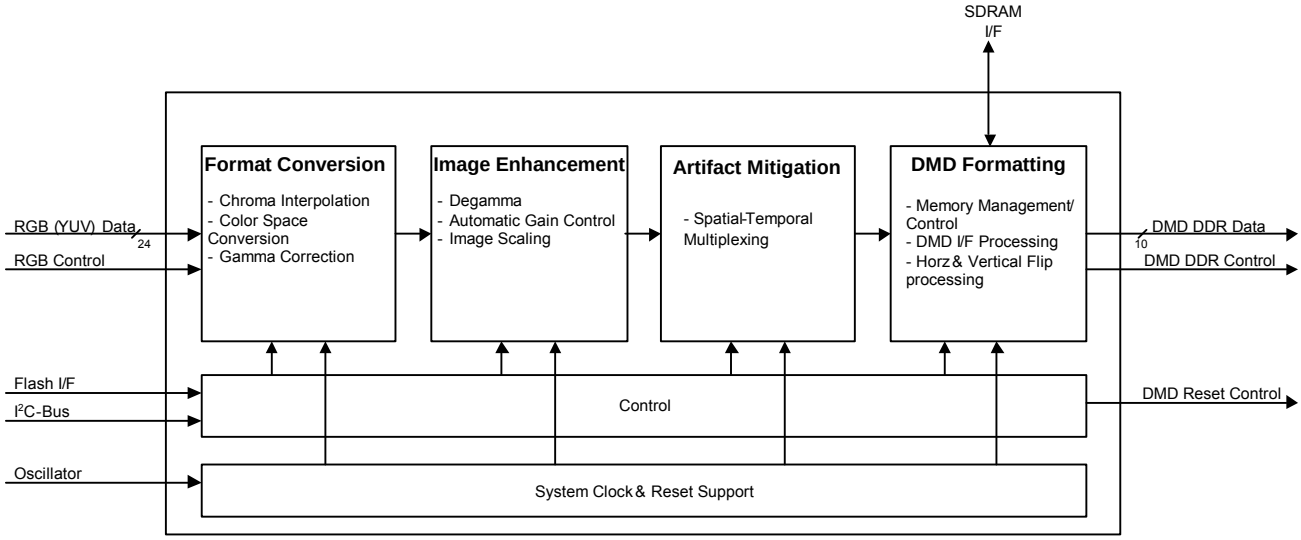
The DPP1505 is the DLP Pico™ Processor meant for use in a standalone Pico Projector. The DPP1505 performs all the image processing and control, along with DMD data formatting, for controlling a 0.17 HVGA DMD.

As with prior DLP® electronics solutions, image data is 100% digital from the DPP1505 input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DPP1505 processes the digital input image and converts the data into a format needed by the DMD. The DMD then reflects light to the screen using binary Pulse-Width-Modulation (PWM) for each pixel mirror. The viewer's eyes integrate this light to form brilliant, crisp images.

Commands can be input to the DPP1505 over the CPU Bus or over an I2C interface.

The digital input interface switching levels, for both image and command inputs, are nominally 1.8V, 2.5V, or 3.3V. The switching level used is selected by setting pin INTFPWR to 1.8V, 2.5V, or 3.3V. The input image interface and I2C interface switching levels must be the same.

Functional Block Diagram



PROJECTOR IMAGE PORT SIGNAL SHARING

The DPP1505 provides a single input port for graphics and motion video inputs. The signals listed below support three input interface modes. Thus some signals have different uses depending on the input interface mode being used.

Below are the three input image interface modes, signal descriptions, and pins needed on the DPP1505. The **SIGNAL FUNCTIONAL DESCRIPTIONS** tables below describe all the signals in the DPP1505.

- BT.656, 9 pins
  - PDATA(7-0) – **P**rojector **Data**
  - PCLK – **P**rojector **Cl**oc**k** (rising edge to capture input data)
- CPU Bus (80-system type), 20 pins or 22 pins
  - PDATA(15-0) or PDATA(17-0) – **P**rojector **Data** (unidirectional, input only)
  - CS – Projector **C**hip **S**elect (active low)
  - WE – Projector **W**rite **E**nable (rising edge to capture input data)
  - CMD – Projector **Co**mman**d** (active low for command, active high for image)
  - CPUVSYNC – **CPU V**ertical **Sync**
- Parallel Bus, 20 pins or 22 pins or 28 pins
  - PDATA(15-0) or PDATA(17-0) or PDATA(23-0) – **P**rojector **Data**
  - HSYNC – **H**orizontal **Sync**
  - VSYNC – **V**ertical **Sync**
  - DATEN – **Dat**a **En** (active high)
  - PCLK – **P**rojector **Cl**oc**k** (rising edge, or falling edge, to capture input data)

SIGNAL FUNCTIONAL DESCRIPTIONS

This section describes the input/output characteristics of signals that interface to the DPP1505 by functional groups. Signals are referenced by names shown in the Pico Projector Formatter Reference Schematic, TI drawing 2509552. The voltage characteristics of various I/O types are described below.

Terminal		I/O	Clock	DEVICE PROGRAMMING
Name	**No.**	**Type**	**System**	**DESCRIPTION**
CFG_DATA	H2	I_1	CFG_DCLK	Data input from an external serial configuration device. Provides configuration data for the device.
CFG_CSZ	D2	O_1	CFG_DCLK	Chip Select Output for an external serial configuration device. Active low.
CFG_DCLK	H1	O_1	CFG_DCLK	Configuration data clock.
CFG_ASDO	C1	O_1	CFG_DCLK	Serial Data Output. This pin sends address and control information to the external PROM during configuration.
MESL_2 MESL_1 MESL_0	G12 H12 H13	I_1	Asynch	Configuration Mode Selection signals.
CEZ	J3	I_1	Asynch	Chip Enable. Active low.
CFGZ	H5	I_1	Asynch	Configuration control. Configuration will start when a low to high transition is detected at this pin.
NSTATUS	F4	B_1	CFG_DCLK	Configuration status pin.
CFG_DONE	H14	B_1	CFG_DCLK	Configuration Done status pin. Signal goes high at the end of configuration.

Terminal		I/O	Clock	BOARD LEVEL TEST & DEBUG
Name	No.	Type	System	DESCRIPTION
JTAG_TDI	H4	I_2	JTAG_TCK	JTAG, Serial Data In.
JTAG_TCK	H3	I_3	N/A	JTAG, Serial Data Clock.
JTAG_TMS	J5	I_2	JTAG_TCK	JTAG, Test Mode Select.
JTAG_TDO	J4	O_1	JTAG_TCK	JTAG, Serial Data Out.

Terminal		I/O	Clock	SYSTEM INTERFACES
Name	No.	Type	System	DESCRIPTION
CLK_IN	E16	I_4	N/A	Input Oscillator Clock (60 MHz)
RESETZ	L8	I_5	Async	Device Reset (Active Low)
PWRGOOD	T3	I_5	Async	System Power Good indicator.
P_SCL	R3	B_2	N/A	I2C Clock
P_SDA	L3	B_2	N/A	I2C Data
I2C_ADDR_SEL	R9	I_4	Async	I2C Address Selection
CPUIF_ENABLE	M16	I_4	Async	CPU I/F command enable for configuration registers access (Should be tied low (Disabled) for DPP1505)
LOW_BAT	G15	I_4	Async	Not Used. Pin reserved for future use.

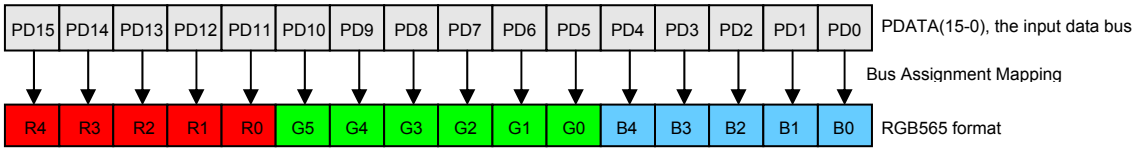
Terminal		I/O	Clock	TEST/DEBUG INTERFACES
Name	No.	Type	System	DESCRIPTION
SpareIn_B8	B8	$I_{1,4,5}$	N/A	Reserved for Test
SpareIn_B9	B9			
SpareIn_E1	E1			
SpareIn_E15	E15			
SpareIn_E2	E2			
SpareIn_M1	M1			
SpareIn_M15	M15			
SpareIn_M2	M2			
SpareIn_A9	A9			
SpareIn_T9	T9			
TEST0	P6	$O_{1,3,4}$	N/A	Reserved for Test Outputs
TEST1	P11			
TEST2	P14			
TEST3	L14			
TEST4	J13			
TEST5	J15			
TEST6	J16			
TEST7	D16			
TEST8	G16			
TEST9	F14			
TEST10	D15			
TEST11	C16			
TEST12	C11			
TEST13	C15			

TEST14	B16			
TEST15	F13			
TEST16	D1			
TEST17	F16			
TEST18	F15			
TEST19	G15			
TEST20	G1			
TEST21	M8			
TEST22	N8			

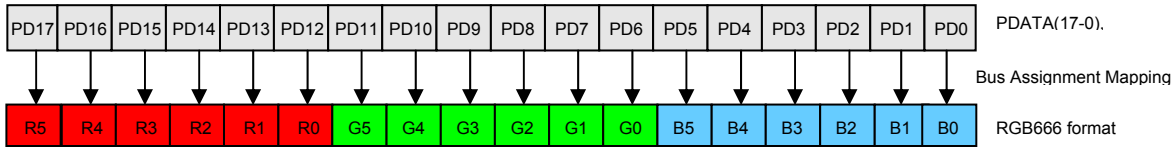
Terminal		I/O	Clock	MAIN VIDEO DATA & CONTROL		
				DESCRIPTION		
Name	**No.**	**Type**	**System**	**Parallel RGB**	**BT.656**	**CPU I/F**
PCLK	R8	I_5	N/A	Clock	Clock	Read enable (Not used)
VSYNC_WE	T5	I_6	PCLK	Vsync	Unused	Write enable (active low)
HSYNC_CS	R4	I_6	PCLK	Hsync	Unused	Chip select (active low)
DATEN_CMD	N3	I_6	PCLK	Active data	Unused	RA0 (active low)
CPUVSYNC	T4	O_5	PCLK	Unused	Unused	TE sync
PDATA[0]	T2	I_5	PCLK	Data*	Data0	Data*
PDATA[1]	R5	I_5	PCLK	Data*	Data1	Data*
PDATA[2]	P2	I_5	PCLK	Data*	Data2	Data*
PDATA[3]	N5	I_5	PCLK	Data*	Data3	Data*
PDATA[4]	N2	I_5	PCLK	Data*	Data4	Data*
PDATA[5]	P8	I_5	PCLK	Data*	Data5	Data*
PDATA[6]	L2	I_5	PCLK	Data*	Data6	Data*
PDATA[7]	T7	I_5	PCLK	Data*	Data7	Data*
PDATA[8]	K2	I_5	PCLK	Data*	Unused	Data*
PDATA[9]	R7	I_5	PCLK	Data*	Unused	Data*
PDATA[10]	J2	I_5	PCLK	Data*	Unused	Data*
PDATA[11]	M7	I_5	PCLK	Data*	Unused	Data*
PDATA[12]	R1	I_5	PCLK	Data*	Unused	Data*
PDATA[13]	L7	I_5	PCLK	Data*	Unused	Data*
PDATA[14]	P1	I_5	PCLK	Data*	Unused	Data*
PDATA[15]	M6	I_5	PCLK	Data*	Unused	Data*
PDATA[16]	N1	I_5	PCLK	Data*	Unused	Data*
PDATA[17]	N6	I_5	PCLK	Data*	Unused	Data*
PDATA[18]	L1	I_5	PCLK	Data*	Unused	Data*
PDATA[19]	P3	I_5	PCLK	Data*	Unused	Data*
PDATA[20]	K1	I_5	PCLK	Data*	Unused	Data*
PDATA[21]	R6	I_5	PCLK	Data*	Unused	Data*
PDATA[22]	J1	I_5	PCLK	Data*	Unused	Data*
PDATA[23]	T6	I_5	PCLK	Data*	Unused	Data*

* 24-bit data is mapped according to rgb565/rgb666/rgb888 pixel format. See following Figures.

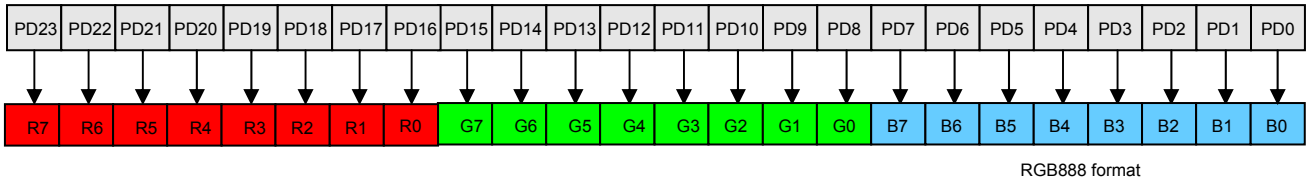
16-bit Input Bus, RGB565 (for CPU or Parallel bus)



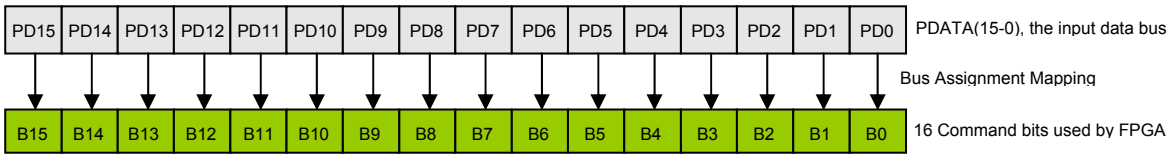
18-bit Input Bus, RGB666 (for CPU or Parallel bus)



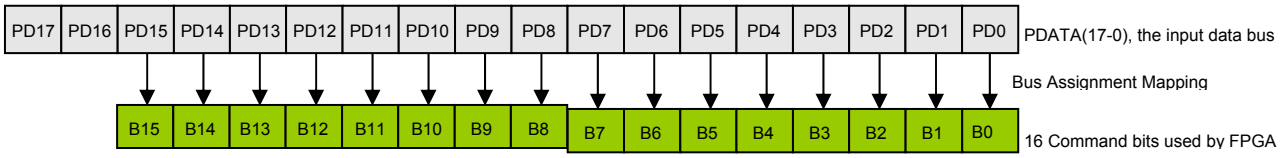
24-bit Input Bus, RGB888 (for Parallel bus only)



CPU I/F Command Bits Used for a 16-bit Data:



CPU I/F Command Bits Used for an 18-bit Data



PDATA17 and PDATA16 are ignored for CPU Command input Commands.

Terminal		I/O	Clock	DMD INTERFACE
Name	No.	Type	System	DESCRIPTION
DMD_D0	P9	O_3	DMD_CLK	DMD Data Pins. DMD Data pins are DDR (Double Data Rate) signals that are clocked on both edges of DMD_DCLK
DMD_D1	R16			
DMD_D2	R13			
DMD_D3	R12			
DMD_D4	R11			
DMD_D5	L15			
DMD_D6	J14			
DMD_D7	L13			
DMD_D8	N16			
DMD_D9	N15			
DMD_DCLK	N12	O_3	N/A	DMD Data clock.
DMD_LOADB	N9	O_3	DMD_CLK	DMD Data Serial Control Signal.
DMD_SCTRL	P16	O_3	DMD_CLK	DMD Data Load Signal.
DMD_TRC	T10	O_3	DMD_CLK	DMD Data Toggle Rate Control.
DMD_A0	T11	O_3	DMD_CLK	DMD Reset Address.
DMD_A1	T14			
DMD_A2	T12			
DMD_SEL0	K16	O_3	DMD_CLK	DMD Reset Selection.
DMD_SEL1	T15			
DMD_MODE	R10	O_3	DMD_CLK	DMD Reset Mode.
DMD_STROBE	T13	O_3	DMD_CLK	DMD Reset Strobe.
DMD_SACBUS	L16	O_3	DMD_CLK	DMD Serial Bus Data.
DMD_SACCLK	K15	O_3	DMD_CLK	DMD Serial Bus Clock.
DMD_OEZ	R14	O_3	DMD_CLK	DMD Reset Output Enable.
DMD_PWR_EN	G5	O_3	N/A	DMD Power Regulator Enable.
RESERVED	H16	O_3	N/A	Pin reserved for future use.
RESERVED	H15	I_4	N/A	Not Used. Pin reserved for future use.

Terminal		I/O	Clock	SDRAM INTERFACE
Name	No.	Type	System	DESCRIPTION
MEM_A0	D12	O_2	MEM_CLK	Multiplexed Row and Column address for the SDRAM.
MEM_A1	B12			
MEM_A2	B14			
MEM_A3	C14			
MEM_A4	D14			
MEM_A5	A15			
MEM_A6	A13			
MEM_A7	B13			
MEM_A8	A14			
MEM_A9	B3			
MEM_A10	A12			
MEM_A11	D11			
MEM_BA0	B11	O_2	MEM_CLK	Bank select for the SDRAM.
MEM_BA1	A11			
MEM_RASZ	C9	O_2	MEM_CLK	Row Address Strobe. Active low.
MEM_CASZ	D9	O_2	MEM_CLK	Column Address Strobe. Active low.
MEM_CKE	E9	O_2	MEM_CLK	Clock Enable. Active high.
MEM_CSZ	B10	O_2	MEM_CLK	Chip Select. Active low.
MEM_HDQM	A10	O_2	MEM_CLK	Data Mask High Byte.
MEM_LDQM	D8	O_2	MEM_CLK	Data Mask Low Byte
MEM_WEZ	F8	O_2	MEM_CLK	Write Enable. Active low.
MEM_CLK	F9	O_2	N/A	Memory Clock. Generated by internal PLL. 100 MHz
MEM_DQ0	A3	B_3	MEM_CLK	Bidirectional data for the SDRAM.
MEM_DQ1	B4			
MEM_DQ2	A5			
MEM_DQ3	A6			
MEM_DQ4	B6			
MEM_DQ5	E6			
MEM_DQ6	A7			
MEM_DQ7	C8			
MEM_DQ8	E8			
MEM_DQ9	B7			
MEM_DQ10	E7			
MEM_DQ11	A2			
MEM_DQ12	D6			
MEM_DQ13	B5			
MEM_DQ14	D5			
MEM_DQ15	A4			

Terminal		I/O	Clock	LED DRIVER INTERFACE
Name	No.	Type	System	DESCRIPTION
BLU_PWM	C6	O_3	CLK_IN	Blue LED PWM signal used to control the LED Current.
RED_PWM	C3	O_3	CLK_IN	Red LED PWM signal used to control the LED Current.
GRN_PWM	D3	O_3	CLK_IN	Green LED PWM signal used to control the LED Current.
BLU_STROBE	F1	O_1	CLK_IN	Blue LED Enable.
RED_STROBE	G2	O_1	CLK_IN	Red LED Enable.
GRN_STROBE	F2	O_1	CLK_IN	Green LED Enable.
LED_FAULTZ	A8	I_4	Async	LED Fault indication. Signal forces LEDDRV_ON low and RGB Strobes low
LED_ENABLE	T8	I_5	Async	LED Enable. Signal forces LEDDRV_ON low and RGB Strobes low.
LEDDRV_ON	F3	O_1	CLK_IN	LED Driver Enable.
RESERVED	B1	I_1	Async	Not used. Reserved for future Use.
RESERVED	C2	O_1	Async	Not used. Reserved for future Use.

	I/O	Clock	IMPEDANCE CONTROL
Name	Type	System	DESCRIPTION
RUP2	PWR	N/A	Bank 4 Control
RDN2	PWR	N/A	Bank 4 Control
RUP3	PWR	N/A	Bank 5 Control
RDN3	PWR	N/A	Bank 5 Control
RUP4	PWR	N/A	Bank 7 Control
RDN4	PWR	N/A	Bank 7 Control

Note: To see how these are connected, see the reference schematic

	I/O	Clock	POWER AND GROUND
Name	Type	System	DESCRIPTION
P1P2V	PWR	N/A	1.2 Volt Core Power.
P2P5V_DPLL	PWR	N/A	2.5 Volt Filtered Power for internal PLL.
P1P8V	PWR	N/A	1.8 Volt I/O Power.
P2P5V	PWR	N/A	2.5 Volt I/O Power.
P3P3V	PWR	N/A	3.3 Volt I/O Power.
GND	PWR	N/A	Common Digital Ground.
GNDA	PWR	N/A	Common PLL Ground.

Note: To see how these are connected, see the reference schematic

I/O Characteristics

All inputs/outputs are of type LVCMOS. The various I/O types supported, as well as their voltage characteristics, are listed in the table below.

I/O Type	Description	VCCIO	VIL (min)	VIL (max)	VIH (min)	VIH (max)	VOL (max)	VOH (min)	Internal pull up/down
I_1	Input	2.5	-0.3	0.8	1.7	VCCIO+0.3			No
I_2	Input	2.5	-0.3	0.8	1.7	VCCIO+0.3			Up
I_3	Input	2.5	-0.3	0.8	1.7	VCCIO+0.3			Down
I_4	Input	1.8	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO+0.3			No
I_5	Input	1.8-3.3	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO+0.3			No
I_6	Input	1.8-3.3	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO+0.3			Up
O_1	Output 8mA	2.5					0.4	2.0	No
O_2	Output 4mA	1.8					0.45	VCCIO – 0.45	No
O_3	Output 8mA	1.8					0.45	VCCIO – 0.45	No
O_4	Output 4mA	1.8-3.3					0.45	VCCIO – 0.45	No
B_1	Bi-directional output, open drain	2.5	-0.3	0.8	1.7	VCCIO+0.3	0.4		No
B_2	Bi-directional output, open drain	1.8-3.3	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO+0.3	0.45		No
B_3	Bi-directional output, 4mA	1.8	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO+0.3	0.45	VCCIO – 0.45	No

Entries in this table are for reference only. Refer to the latest version of the Altera Cyclone III Device Handbook for the latest update on I/O voltage characteristics.

Power and Ground Pins

Power and Ground connections to the DPP1505 are made up of three categories:

1) Input power and ground pins.
2) Input signals which are tied to a fixed level.
3) Cyclone III devices support on-chip series termination with calibration in all banks. The on-chip series termination calibration circuit compares the total impedance of the I/O buffer to the external 25 Ω ±1% or 50 Ω ±1% resistors connected to the RUP and RDN pins, and dynamically adjusts the I/O buffer impedance until they match. OCT with calibration is achieved using the OCT calibration block circuitry. There is one OCT calibration block in bank 2, 4, 5, and 7. Each calibration block supports each side of the I/O banks. Since there are two I/O banks sharing the same calibration block, both banks must have the same VCCIO if both banks enable OCT calibration. If two related banks have different VCCIOs, only the bank where the calibration block resides can enable the OCT calibration.

Category	Name	Description	Pin Number
1	VCC12	1.2V power supply for core logic	F7, F11, G6, G7, G8, G9, G10, H6, H11, J6, J12, K7, K9, K10, K11, L6, M9, M11
1	VCC25_DPLL	2.5V power supply for internal PLLs	F5, F12, L5, L12
1	VCCIO18	1.8V power supply for I/Os on Banks 4-8	A1, A16, C4, C7, C10, C13, E14, G14, K14, M14, P10, P13, T16
1	FLASHPWR	2.5V or 3.3v power supply for Bank I/Os (Serial Configuration FLASH Interface) Bank 1	E3, G3
1	INTFPWR	1.8V, 2.5V or 3.3V power supply for I/Os on Video Interface Banks 2-3	K3, M3, P4, P7, T1
1	VCCD_PLL1-4	1.2V power supply for DLL	N4, D13, D4, N13
1	GND	Common ground	B2, B15, C5, C12, D7, D10, E4, E13, F6, F10, G4, G11, G13, H7, H8, H9, H10, J7, J8, J9, J10, J11, K4, K6, K8, K12, K13, L9, L10, L11, M4, M13, N7, N10, P5, P12, R2, R15
1	GNDA1-4	Analog Ground	M5, E12, E5, M12
2	GND	Virtual GND output pins that are driven to a low level for noise reduction.	-none-
3	RDN1, RUP1	Bank 2 - Not connected	L4, K5
3	RDN2, RUP2	Bank 4 DMD interface support	N11, M10
3	RDN3, RUP3	Bank 5 DMD interface support	P15, N14
3	RDN4, RUP4	Bank 7 & 8 memory interface support	E10, E11

Note: To see how these are connected, see the reference schematic

VIDEO INPUT PIXEL INTERFACE

Timing Requirements

NO.		PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
1	f_{clock}	Clock frequency, PCLK		1	28	MHz
2	t_t	Transition time, $t_t = t_f / t_r$ PCLK	20% to 80% reference points (signal)		1.0	ns
3	$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	11		ns
4	$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	11		ns
5	t_j	Clock Period Jitter, PCLK			See Note 2	ns
6	t_{su}	Setup time, PDATA(23-0) valid before PCLK	See Note 1	3.0		ns
7	t_h	Hold time, PDATA(23-0) valid after PWCLK	See Note 1	3.0		ns
8	t_{su}	Setup time, VSYNC_WE valid before PCLK	See Note 1	3.0		ns
9	t_h	Hold time, VSYNC_WE valid after PCLK	See Note 1	3.0		ns
10	t_{su}	Setup time, HSYNC_CS valid before PCLK	See Note 1	3.0		ns
11	t_h	Hold time, HSYNC_CS valid after PCLK	See Note 1	3.0		ns
12	t_{su}	Setup time, DATEN_CMD valid before PCLK	See Note 1	3.0		ns
13	t_h	Hold time, DATEN,_CMD valid after PCLK	See Note 1	3.0		ns

NOTES:
1) PCLK may be inverted from that show in the figure below. In that case the same specifications in the table are valid except now referenced to the falling edge of the clock. If the falling edge of PCLK is to be used, an I2C command is needed to tell the DPP1505 to using the falling edge of PCLK.
2) Use the following formula to obtain the jitter. Jitter = [1/frequency – 30 ns]. Setup and Hold must still be met.

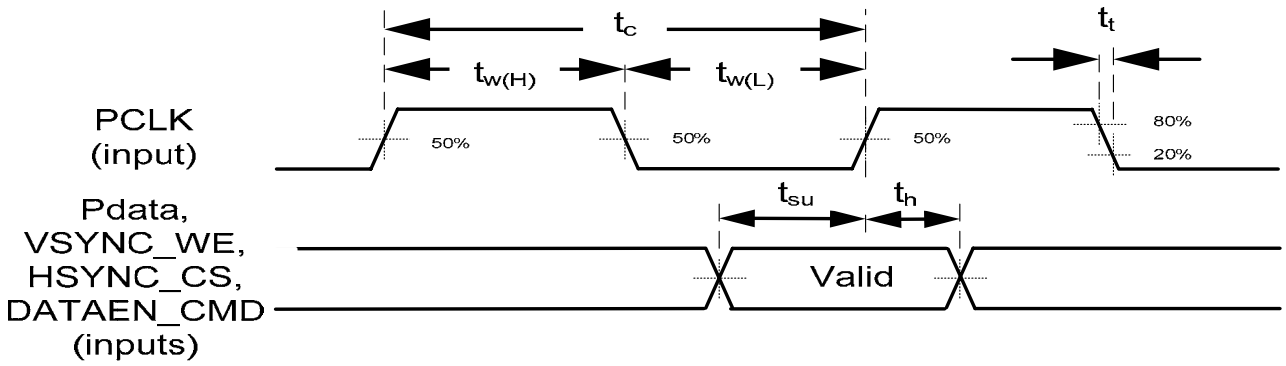


Figure 5 - Input Port Interface

Absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1):	V_{CC12}	-0.5 V to 1.80 V
	V_{CCIO18}	-0.5 V to 3.90 V
	V_{CCA25_DPLL}	-0.5 V to 3.75 V
	INTFPWR	-0.5 V to 3.90 V
	VCCD_PLL1-4	-0.5 V to 1.80 V
Input voltage range, V_I (see Note 2):	1.8 V, 2.5V, 3.3V	–0.5 V to 3.95 V
Continuous total power dissipation:	Typical	0.300 W
Operating junction temperature range, T_J		-40°C to 125°C
Storage temperature range, T_{stg}		–60°C to 150°C
Electrostatic discharge voltage using the human body model		+/- 2000 V
Electrostatic discharge voltage using the charged device model		+/- 500 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

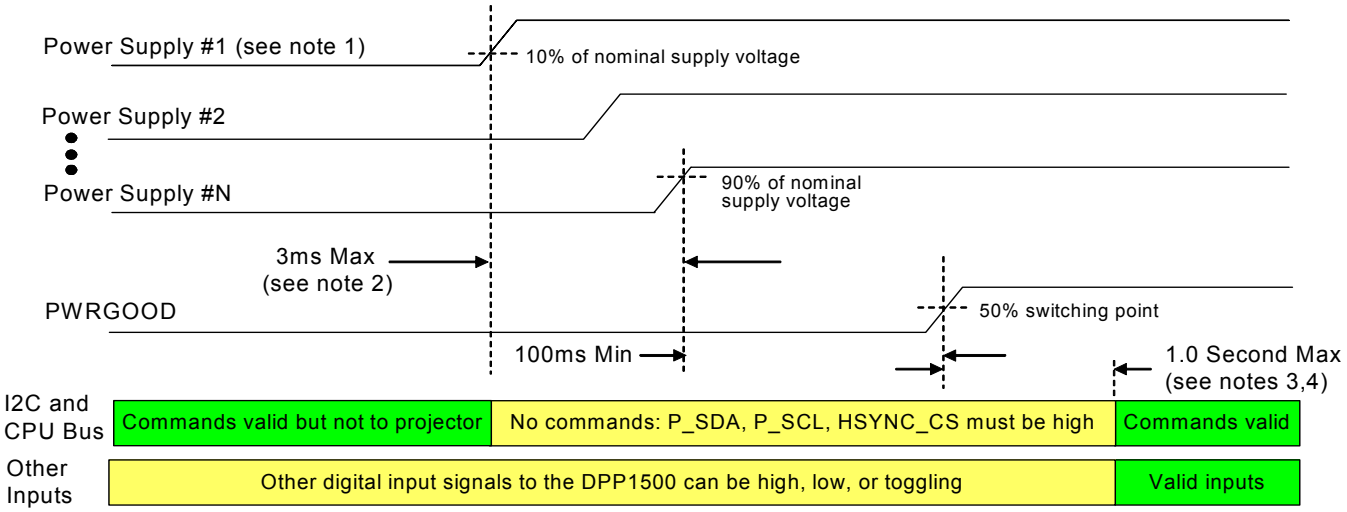
NOTES:1. All voltage values are with respect to GND, and at the device not at the power supply.
2. Applies to external input and bidirectional buffers.

Recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC12	1.2V Supply voltage, core logic		1.15	1.2	1.25	V
VCC18	1.5V Supply voltage, HSTL output buffers		1.71	1.8	1.89	V
VCCA25_DPLL	2.5V Analog Voltage for PLL regulator		2.375	2.5	2.625	V
INTFPWR	At 1.8V IO Rail		1.71	1.8	1.89	V
INTFPWR	At 2.5V IO Rail		2.375	2.5	2.625	V
INTFPWR	At 3.3V IO Rail		3.15	3.3	3.45	V
VCCD_PLL1-4	1.2V Supply voltage, for PLL		1.15	1.2	1.25	V
V_{IH}	High-level Input voltage	1.8V LVCMOS	0.65*VCCIO			V
		2.5V LVCMOS	1.7			
		3.3VLVCMOS	1.7			
V_{IL}	Low-level Input voltage	1.8V LVCMOS			0.35*VCCIO	V
		2.5V LVCMOS			0.8	
		3.3VLVCMOS			0.8	
V_I	Input voltage		-0.5		3.6	V
V_O	Output voltage		0		VCCIO	V
tRamp	Power Supply Ramptime		50 us		3 msec	-
T_J	Operating junction temperature		-20		85	°C

Power Sequencing

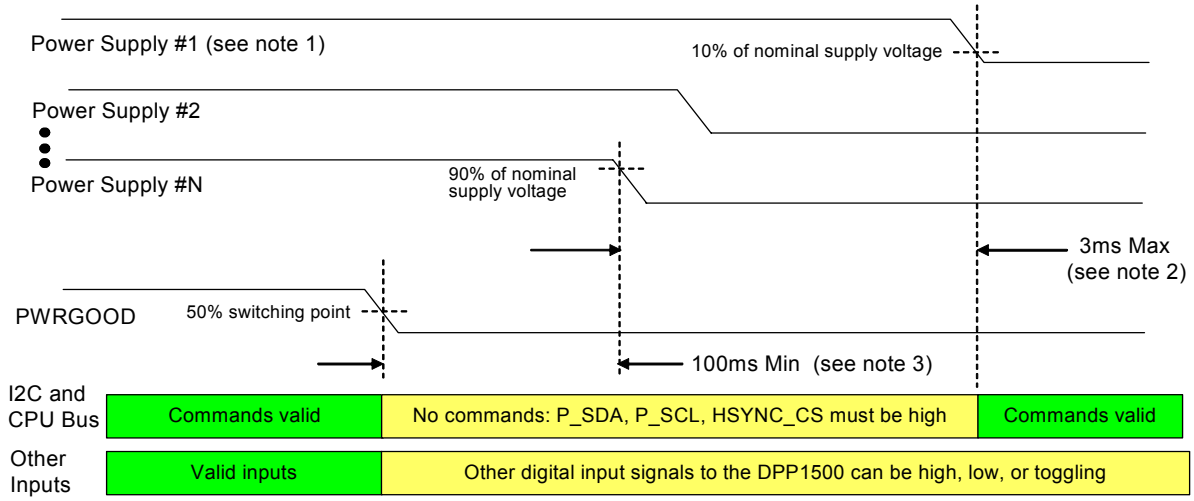
Power-up timing for the PICOEVM1 is shown in Figure 1and Power-down timing is shown in Figure 2, summarizing PICOEVM1 board power-up and power-down timing including the timing for signals DMD_PWR_EN (enables the TPS65120 which creates voltages VRST, VBIAS, and VOFS for the DMD) and LEDDRV_ON (enables the TPS63000 which is the LED Driver's main chip).



NOTES:

1. Power supplies shown above (#1 - #N) are all of the projector power supplies (P2P5V, P1P8V, P1P2V, INTFPWR, FLASHPWR, and P3P3V if the TVP5150 is used). For the LED driver and the DMD power supplies (VRST, VBIAS, VOFS), the projector will internally handle sequencing on of these power supplies as needed.
2. Power supplies (#1 - #N) can sequence on in any order as long they all turn on within a 3ms time window.
3. 1.0 seconds max after PWRGOOD goes high the projector begins to operate using the default configuration settings from Flash. After 1.0 seconds min from PWRGOOD going high, commands can be input to the projector.
4. I2C reads/writes and CPU bus writes to the DPP1500 are invalid during power-up. I2C signals and the CPU bus chip select (HSYNC_CS) should all be high during DPP1500 power-up including for reads/writes to other devices.

Figure 1. Power-Up Power Supply and PWRGOOD Sequencing



NOTES:

1. Power supplies shown above (#1 - #N) are all of the projector power supplies (P2P5V, P1P8V, P1P2V, INTFPWR, FLASHPWR, and P3P3V if the TVP5150 is used). For the LED driver and the DMD power supplies (VRST, VBIAS, VOFS), the projector will internally handle sequencing off these power supplies as needed.
2. Power supplies (#1 - #N) can sequence off in any order as long they all turn off within a 3ms time window.
3. After PWRGOOD goes low, these events occur within the projector:
   - The LEDs are automatically turned off. (An I2C or CPU bus LED disable command is not needed).
   - The DPP1500 will automatically park the DMD mirrors to a flat state. (An I2C or CPU bus park command is not needed.)

Figure 2. Power-Down Power Supply and PWRGOOD Sequencing

SDRAM Memory

The DPP1505 requires an external Mobile SDR SDRAM. The DPP1505 can support either a 128Mbit or a 64Mbit SDRAM. The basic requirements for the SDRAM are:

- SDRAM Type: Mobile SDR
- Speed: 125MHz minimum
- 16-bit interface
- Size: 64Mbit or 128Mbit
- Supply Voltage: 1.8V

Table 1 shows the SDRAM parts that have been tested by TI on the PICOEVM1 board. All have been found to work properly and are therefore recommended for production use with the DPP1505.

Table 1 Supported SDRAM Devices

Part Number	Manufacturer	Size
K4M64163PK-BG750JR	Samsung	64Mbit
K4M28163PH-BG750JR	Samsung	128Mbit
MT48H4M16LFB4-8	Micron	64Mbit
MT48H8M16LFB4-8	Micron	128Mbit

Design Guidelines

The DPP1505 performs specific video formatting functions to an input video stream. When designing with the component set, specific layout guidelines must be followed to ensure that all I/O timing requirements around the component set are met. In addition, the memory interface between the DPP1505 and the external SDRAM is designed to operate at a fixed bandwidth with the assumption that the input pixel clock frequency is within a specific range.

PCB layout guidelines for internal PLL power

The following guidelines are recommended to achieve desired performance relative to the internal PLL:

The DPP1505 contains 1 internal PLL which has a dedicated analog supply (**VCC25_DPLL**). As a minimum, **VCC25_DPLL** power and ground pins should be isolated using an RC-filter consisting of a 100 Ohm series resistor and two capacitors (to widen the spectrum of noise absorption). It's recommended that one capacitor be a 25uf, electrolytic capacitor with good low frequency cut off. Since the filter also needs to sustain its attenuation at high frequencies, the other capacitor should be a 100nf, non-electrolytic capacitor. All three components should be placed as close to the DPP1505 as possible but it's especially important to keep the leads of the high frequency capacitor as short as possible. Note that both capacitors should be connected across VCC_PLL & VSS_PLL but VSS_PLL should not be connected to the common ground. This is the minimum recommendation and additional filtering is encouraged. The series resistor is used to limit DC and thus it should be noted that if a quality series inductor is used, it should not be used without a series resistor as it will not provide the needed DC current limit.

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, **VCC_PLL** must be a single trace from the DPP1505 to the high frequency capacitor, and then to the low frequency capacitor, and then through the series resistor to the power source. The power and ground traces should be as short as possible, parallel to each other and as close as possible to each other.

General handling guidelines for unused CMOS-type pins

To avoid potentially damaging current caused by floating CMOS input-only pins, it is recommended that unused DPP1505 input pins be tied through a pull-up resistor to its associated power supply or a pull-down to ground. For DPP1505 inputs with an internal pull-up or pull-down resistors, it is unnecessary to add an external pull-up/ pull down unless specifically recommended. Note that internal pull-up & pull-down resistors are weak and should not be expected to drive the external line.

Unused output-only pins can be left open.

When possible, it is recommended that unused Bi-directional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or down) using an appropriate resistor.

Mobile-SDR Memory and DMD Interface Considerations

High Speed Interface waveform quality and timing on the DPP1505 ASIC (i.e. the Mobile SDR Memory I/F and the DMD Interface) are dependent on the total length of the interconnect system, the spacing between traces, the characteristic

impedance, etch losses, and how well matched the lengths are across the interface. Thus ensuring positive timing margin requires attention to many factors.

As an example, DMD Interface system timing margin can be calculated as follows:
Setup Margin = (DPP1505 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)
Hold-time Margin = (DPP1505 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

Where PCB SI degradation is signal integrity degradation due to PCB affects which includes such things as Simultaneously Switching Output (SSO) noise, cross-talk and Inter-symbol Interference (ISI) noise.

DPP1505 I/O timing parameters as well as Mobile-SDR and DMD I/O timing parameters can be easily found in their corresponding datasheets. Similarly, PCB routing mismatch can be easily budgeted and met via controlled PCB routing. However PCB SI degradation is not so straight forward.

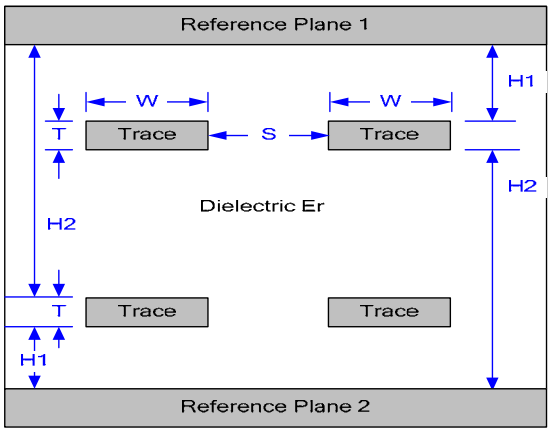
In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that will satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work but should be confirmed with PCB signal integrity analysis or lab measurements.

PCB design:

- Configuration: Asymmetric Dual Stripline
- Etch Thickness (T): 0.5 oz copper
- Single-Ended Signal Impedance: 50 ohms (+/- 10%)
- Differential Signal Impedance: 100 ohms differential (+/- 10%)

PCB stackup:

- Reference plane 1 is assumed to be a ground plane for proper return path
- Reference plane 2 is assumed to be the I/O power plane or ground
- Dielectric FR4, (Er): 4.2 (nominal)
- Signal trace distance to reference plane 1 (H1): 5.0 mil (nominal)
- Signal trace distance to reference plane 2 (H2): 34.2 mil (nominal)



PCB Stackup Geometries

General PCB routing (Applies to all corresponding PCB signal):

Parameter	Application	Single Ended Signals	Differential Pairs	Unit
Line width (W)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB Etch Data/ Control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB Etch Clocks	7 (0.18)	4.25 (0.11)	mil (mm)
Differential signal pair spacing (S)	PCB Etch Data/ Control	n/a	5.75 [1] (0.15)	mil (mm)
	PCB Etch Clocks	n/a	5.75 [1] (0.15)	mil (mm)
Minimum Line spacing to other signals (S)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB Etch Data/ Control	10 (0.25)	20 (0.51)	mil (mm)
	PCB Etch Clocks	20 (0.51)	20 (0.51)	mil (mm)
Maximum Differential pair P-to-N length mismatch	Total Clock	n/a	12 (0.3)	mil (mm)

1. Spacing may vary to maintain differential impedance requirements

Maximum, pin to pin, PCB interconnects etch lengths:

Bus	Signal Interconnect Topology		Unit
	Single Board Signal routing length	**Multi-Board Signal routing length**	
DMD: DMD_D(14:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OEZ DMD_DAD_STRB, DMD_DAD_BUS, DMD_SAC_CLK & DMD_SAC_BUS	4.0 101.5 max	3.5 88.91 max	inch mm
Mobile SDR: MEM0_DQ(15:8), MEM0_HDQM	1.5 max 38.1 max	NA	inch mm
MobileSDR: MEM0_DQ(7:0), MEM0_LDQM	1.5 max 38.1 max	NA	inch mm
MobileSDR: MEM0_CLK, MEM0_A(11:0), MEM0_BA(1:0), MEM0_CKE, MEM0_CSZ, MEM0_RASZ, MEM0_CASZ & MEM0_WEZ	2.5 max 63.5 max	N/A	inch mm

Notes:
1. Max signal routing length includes escape routing
2. Multi-board DMD routing length is more restricted due to the impact of the connector

I/F Specific PCB routing:

Signal Group length Matching				
I/F	**Signal Group**	**Reference Signal**	**Max Mismatch**	**Unit**
DMD	DMD_D(14:0), DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OEZ	DMD_DCLK	+/- 500 (+/- 12.7)	mil (mm)
DMD	DMD_DAD_STRB, DMD_DAD_BUS	DMD_DCLK	+/- 750 (+/- 19.05)	mil (mm)
DMD	DMD_SAC_BUS	DMD_SAC_CLK	+/- 750 (+/- 19.05)	mil (mm)
DMD	DMD_SAC_CLK	DMD_DCLK	+/- 500 (+/- 12.7)	mil (mm)

Notes:

1. The above values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DPP1505, the DMD or the mSDR memory.
2. DMD data and control lines are double data rate where as DMD_SAC & DMD_DAD lines are single data rate. Matching of the double data rate lines is more critical and should take precedence over matching single data rate lines.

Number of layer changes:

- Single Ended signals: Minimize the number of layer changes
- Differential signals: Individual differential pairs can be routed on different layers but the signals of a given pair should not change layers.

Stubs:

- Stubs should be avoided

Termination Requirements:

DMD I/F: All DMD I/F signals, with the exception of DMD_OEZ (Specifically DMD_D(14:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_DAD_STRB, DMD_DAD_BUS, DMD_SAC_CLK & DMD_SAC_BUS), should be series terminated at the source with a 30 Ohm series resistor.

Routing Notes:

- The data lines and LOADB, OEZ, BUS,TRC, STRB SCTRL need to be equal length from the DPP1505 to the DMD plus or minus 0.500”.
- Clock needs to be equal to the mean of the shortest and longest data line.
- SACCLK and SACBUS should be equal length within 0.500”.

Package Information

The DPP1505 is packaged in a 256-pin Non-Thermally Enhanced Ultra Fineline Ball-Grid Array. Refer to the Altera Cyclone III Device Handbook for detail of package information, http://www.altera.com/literature/ds/256-UBGA.pdf .

General Electrical Requirements Tables

Estimated Power Dissipation

Supply	Typical	Unit
VCC12	122	mA
VCC18	15	mA
VCC25_DPLL	35	mA
INTFPWR	6.3	mA
VCCD_PLL1-4	12.1	mA
FLASH_PWR	5.5	mA

Thermal Considerations

The underlying thermal limitation for the DPP1505 is that the maximum operating junction temperature (TJ) not be exceeded (this is defined in the recommended operating conditions table). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DPP1505 and power dissipation of surrounding components. The DPP1505's package is designed primarily to extract heat through the power & ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

Mechanical Data

The DPP1505 is packaged in a 256-pin Non-Thermally Enhanced Ultra Fineline Ball-Grid Array. Refer to the Altera Cyclone III Device Handbook for detail of package information, http://www.altera.com/literature/ds/256-UBGA.pdf .

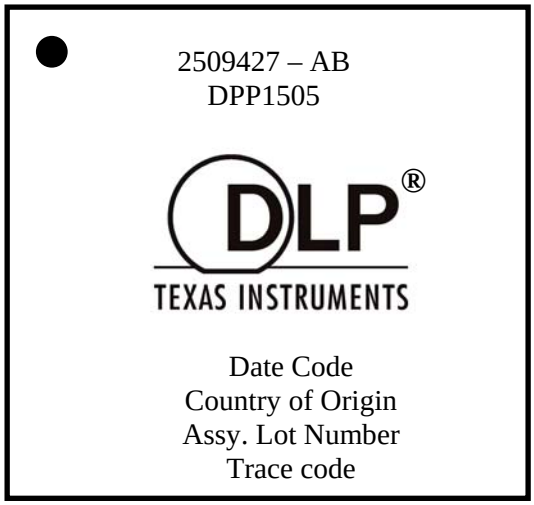
Device Marking

Device Marking should be done as shown below.

INK MARK
TOPSIDE INFORMATION
CENTER JUSTIFY

FONT TYPE: NEWS GOTHIC	
TEXT HEIGHT:	0.028”
TEXT SPACING:	0.010
TEXT TO LOGO SPACING:	0.030”
DLP LOGO HEIGHT:	0.127”
® SYMBOL HEIGHT:	0.030”
LOGO SPACING:	0.040”
TEXT HEIGHT:	0.028”
TEXT SPACING:	0.020”
LOT # TEXT HEIGHT:	0.028”
TRACE CODE HEIGHT:	0.028”

NOTE: DRAWING NOT TO SCALE



Marking Definitions:

Line 1 : TI Part Number
AB (1 or 2 numeric) = ‘A’ corresponds to the TI device dash number. ‘B’ is reserved for unqualified device marking. All unqualified device, including prototypes and skew lot samples, are labeled with the letter “X” in the ‘B’ marking location (following the TI part number). ‘B’ is left blank for qualified devices.
Line 2 : Device Name
Line 3 : DLP® logo
Line 4 : Date Code
Line 5 : Country of Origin
Line 6 : Assembly Lot Number
Line 7 : Trace Code

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